Installation Guide

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For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E8019A Analysis Probe for HITACHI SH7709

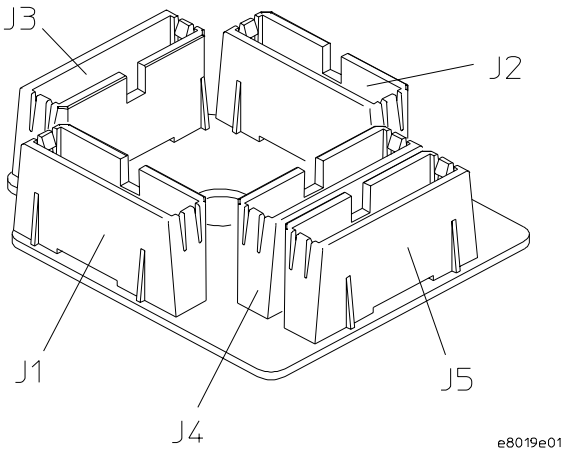
The HP E8019A Analysis Probe — At a Glance

The HP E8019A Analysis Probe provides a complete interface for state or timing analysis between any SH7709 target system and the following HP logic analyzers:

- HP 16600A
- HP 16601A
- HP 16602A
- HP 16550A (one or two cards)
- HP 16555A/D (two or three cards)
- HP 16556A/D (two or three cards)
- HP 16557D (two or three cards)

The Analysis Probe provides the physical connection between the target microprocessor and the logic analyzer. The configuration software sets up the logic analyzer for compatibility with the Analysis Probe. The Emulation Interface Software allows you to obtain displays of the microprocessor operations in SH7709 mnemonics or C-source.

For additional information on the supported logic analyzers or microprocessors, refer to the appropriate reference manuals for those products.



HP E8019A Analysis Probe

In This Book

This book is the installation guide for the HP E8019A Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This installation guide is organized into three chapters:

Chapter 1 explains how to attach the Analysis Probe to the target and how to configure the logic analyzer for state and/or timing analysis.

Chapter 2 provides reference information on the format specification and symbols configured by the Analysis Probe software and information about the inverse assemblers and status encoding.

Chapter 3 contains reference information on the Analysis Probe hardware, including the characteristics and signal mapping for the Analysis Probe.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

Contents

1

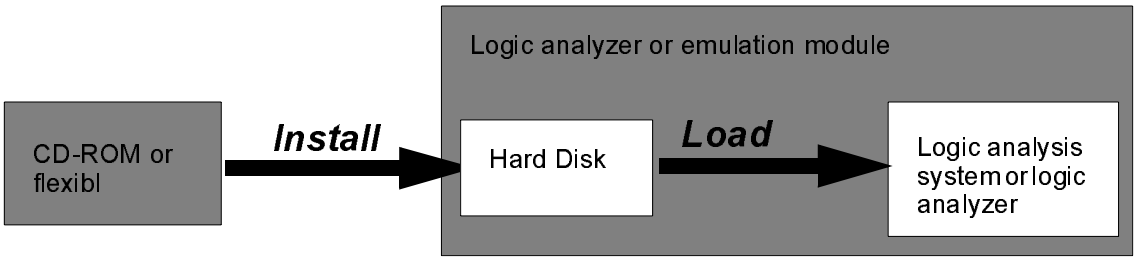
Installing Software

Installing Software

This chapter explains how to install the software you will need for your analysis probe or emulation solution.

Installing and loading

Installing the software will copy the files to the hard disk of your logic anlysis system. Later, you will need to **load** some of the files into the appropriate measurement module.



What needs to be installed

HP 16600A/700A-series logic analysis systems

If you ordered an analysis probe or emulation solution with your logic analysis system, the software was installed at the factory.

The following files are installed when you install a processor support package from the CD-ROM:

- Logic analysis system configuration files
- Personality files for the Setup Assistant

To install the software from CD-ROM (HP 16600A/700A)

Installing a processor support package from a CD-ROM will take just a few minutes. If the processor support package requires an update to the HP 16600A/700A operating system, installation may take approximately 15 minutes.

1 **Insert the CD-ROM in the drive.**

2 **Click the System Admin icon.**

3 **Click Install... .**

Change the media type to "CD-ROM" if necessary.

4 **Click Apply.**

5 **From the list of types of packages, select "PROC-SUPPORT."**

A list of the processor support packages on the CD-ROM will be displayed.

6 **Click on the "SH3" package.**

If you are unsure if this is the correct package, click Details for information on what the package contains.

7 **Click Install... .**

The dialog box will display "Progress: completed successfully" when the installation is complete.

8 **Click Close.**

To list software packages which are installed (HP 16600A/700A)

- In the System Administration Tools window, click **List...** .

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This chapter explains how to set up the HP E8019A Analysis Probehardware, and connect the Analysis Probeto supported logic analyzers.

Before You Begin

This section lists the logic analyzer(s) supported by the HP E8019A and provides other information about the analyzer(s) and the Analysis Probe.

Equipment Supplied

- The HP E8019A SH7709 Analysis Probe, which includes the HP QFP Elastomeric Probing System
- Three HP E5346A High-Density Adapter Cables, and labels.
- A Cam Tool, for separating the Analysis Probefrom the probing system.
- This Installation Guide.
- The HP QFP Elastomeric Probing System Installation Guide.

Minimum Equipment Required

- The HP E8019A SH7709 Analysis Probe, including the HP QFP Elastomeric Probing System.
- Three HP E5346A High-Density Adapter Cables.
- One of the logic analyzers listed in the table on the following page.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16602A	102	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16600A	208	100 MHz	125 MHz	64 k states
16550A (one cards)	102	100 MHz	250 MHz	4 k states
16550A (two cards)	204	100 MHz	250 MHz	4 k states
16555A (two cards)	136	110 MHz	250 MHz	1 M states
16555A (three cards)	204	110 MHz	250 MHz	1 M states
16555D (two cards)	136	110 MHz	250 MHz	2 M states
16555D (three cards)	204	110 MHz	250 MHz	2 M states
16556A (two cards)	136	100 MHz	200 MHz	1M states
16556A (three cards)	204	100 MHz	200 MHz	1M states
16556D (two cards)	136	100 MHz	200 MHz	2 M states
16556D (three cards)	204	100 MHz	200 MHz	2 M states
16557D (two cards)	136	135 MHz	500 MHz	4 M states
16557D (three cards)	204	135 MHz	500 MHz	4 M states

Setting Up the Analysis Probe Hardware

Setting up the Analysis Probehardware consists of the following major steps:

- Turn off the logic analyzer and the target system.
- Connect the Elastomeric Probing System retainer to the target system.
- Attach the Analysis Probecircuit board and adapter to the retainer.
- Attach the labels to the HP E5346A High-Density cables, then connect the cables to the Analysis Probe.
- Connect the logic analyzer pods to the high-density adapter cables.

The remainder of this section describes these general steps in more detail.

Turn off the logic analyzer and the target system

To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. The logic analyzer should always be powered up before the target system. When powering down, power down the target system first and then power down the logic analyzer.

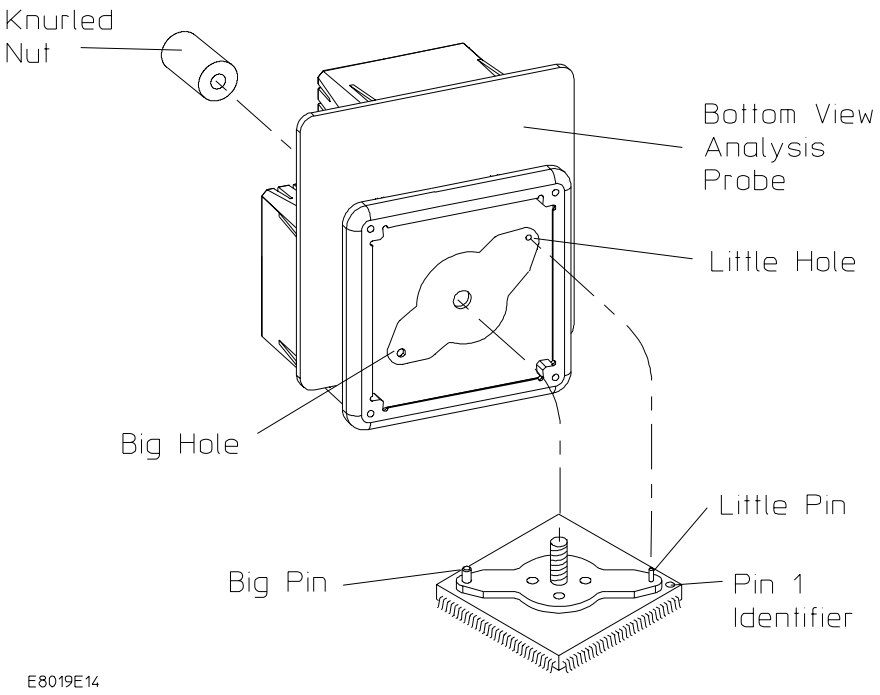
To connect the Analysis Probe to the target system

Use the following steps to connect the Analysis Probeto the target system.

CAUTION **Equipment Damage.** To prevent equipment damage, be sure to remove power from both the target system and the logic analyzer whenever the Analysis Probeis being connected or disconnected.

1. **Turn off the target system and logic analyzer.**
2. **Using the instructions in the *HP QFP Elastomeric Probing System Installation Guide:***
   - Prepare to attach the Retainer to the QFP microprocessor
   - Test the alignment before adhering the Retainer
   - Adhere the Retainer to the QFP microprocessor
   - Install the HP E8019A Analysis Probeas described in "Install the Probe Adapter"
3. **Using the illustration on the next page, note the following indicators:**
   - position of Pin 1 on the microprocessor
   - position of little pin on the retainer
   - position of little hole on the probe adapter

CAUTION Serious damage to the target system or Analysis Probecan result from incorrect connection. Note the position of pin 1 on the target system and Analysis Probeprior to making any connection. Also, take care to align the pins so that all pins are making contact.



Pin 1 Alignment for Target System and Analysis Probe

To disconnect the Analysis Probe from the target system

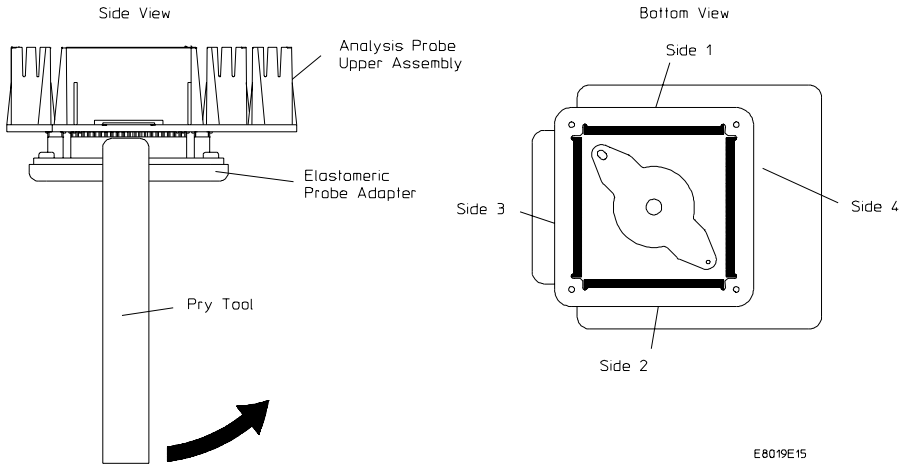
Use the following steps to disconnect the Analysis Probefrom the target system.

1. **Remove power from the target system.**
2. **Remove power from the logic analyzer.**
3. **Unscrew the knurled nut.**
4. **Lift the Analysis Probestraight up.**

To separate the Analysis Probe upper assembly from the probe head

Hewlett-Packard does not recommend separating the Analysis Probeupper assembly from the elastomeric probe head. However, unforeseen circumstances might require you to separate the assembly.

Use the Cam Tool supplied. Insert the tool into the first side as shown in the following illustration, and rotate it until the connectors begin to separate. Repeat this process for the other three sides in consecutive order until the Analysis Probeupper assembly and the elastomeric probe head are separated.

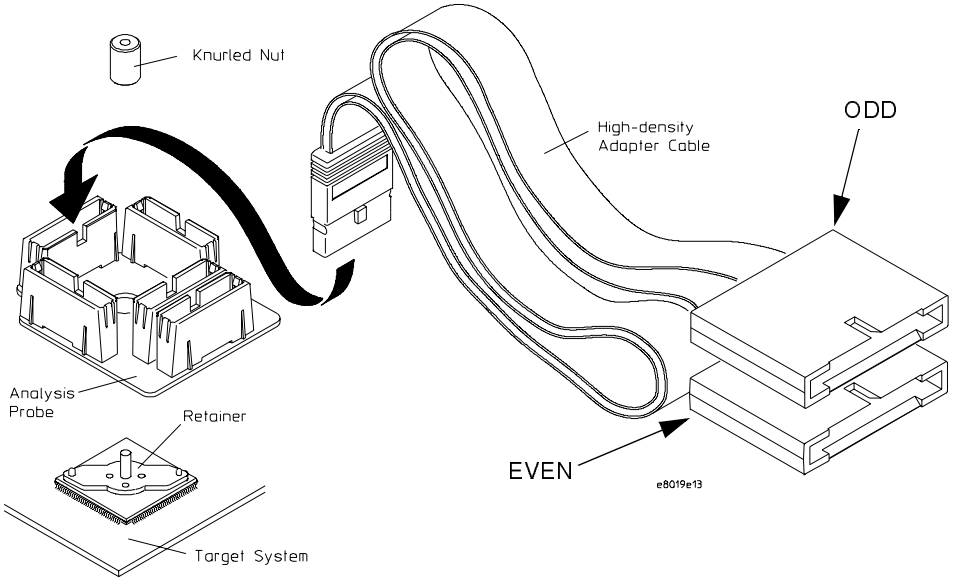


To reconnect Analysis Probe and probe head

Place the elastomeric probe head in its protective cover. Orient the elastomeric probe head and the Analysis Probeupper assembly as shown in the illustration on the previous page. As you begin to insert the pins of the Analysis Probeupper assembly into the sockets on the elastomeric probe head, ensure that all of the pins are engaging. Look closely at both ends of all four sockets to ensure all pins are properly mated. Gently apply pressure until the connectors are fully mated.

To connect the high-density adapter cables to the Analysis Probe

The high-density adapter cables, and labels to identify them, are included with the HP E8019A Analysis Probe. The labels identify the cables by the pod number, and "o" or "e" (for odd or even). Attach the labels to the cables, then connect the cables to the connectors on the Analysis Probeas shown in the following illustrations.



High-Density Adapter Cables

Setting up the Logic Analyzer

Connect the logic analyzer pod cables to the logic analyzer and to the mictor connector on the Analysis Probe. Required number of pods depend on which memory type you are using, how many wait cycles are interleaved, and speed of your target system's CKIO speed. See table below, then refer to the pod diagram for the analyzer you are using.

External Bus Speed	Memory Types Combination			Description	PODs	Minimum Logic Analyser supported	Config File	Connec-tion Type
	Other	EDO	SDRAM					
<=40MHz (*1)(*2)	D.C.	D.C.	D.C.	Any memory combina-tions with external bus speed of 40MHz or slower	6	16602A	SH7709F_0	A
						16700A+16550A	SH7709F_0	B
						16700A+16555/6/7x2(*2)	SH7709M_0	C
> 40MHz (*2)	YES	NO	NO	Any types of memory other than EDO-DRAM or SDRAM	6	16602A	SH7709F_1	A
						16700A+16550A	SH7709F_1	B
						16700+16555/6/7x2(*2)	SH7709M_1	C
	D.C.	YES	NO	EDO-DRAM with any types of memory	8	16601A	SH7709F_2	D
						16700A+16550Ax2	SH7709F_2	E
						16700A+16555/6/7x2(*2)	SH7709M_2	F
	YES (w/wait)	NO	YES	SDRAM with other RAM with wait cycle	8	16601A	SH7709F_3	D
						16700A+16550Ax2	SH7709F_3	E
						16700A+16555/6/7x2(*2)	SH7709M_3	F
	YES (no-wait)	NO	YES	SDRAM with other RAM with no-wait cycle	10	16600A	SH7709F_4	G
						16700A+16550Ax2	SH7709F_4	H
						16700A+16555/6/7x3(*2)	SH7709M_4	I

D.C. = Don't Care

(*1) Condition of <=40MHz : CKIO(cycle) = min25ns, CKIO(low)=min10ns, CKIO(high)=min10ns

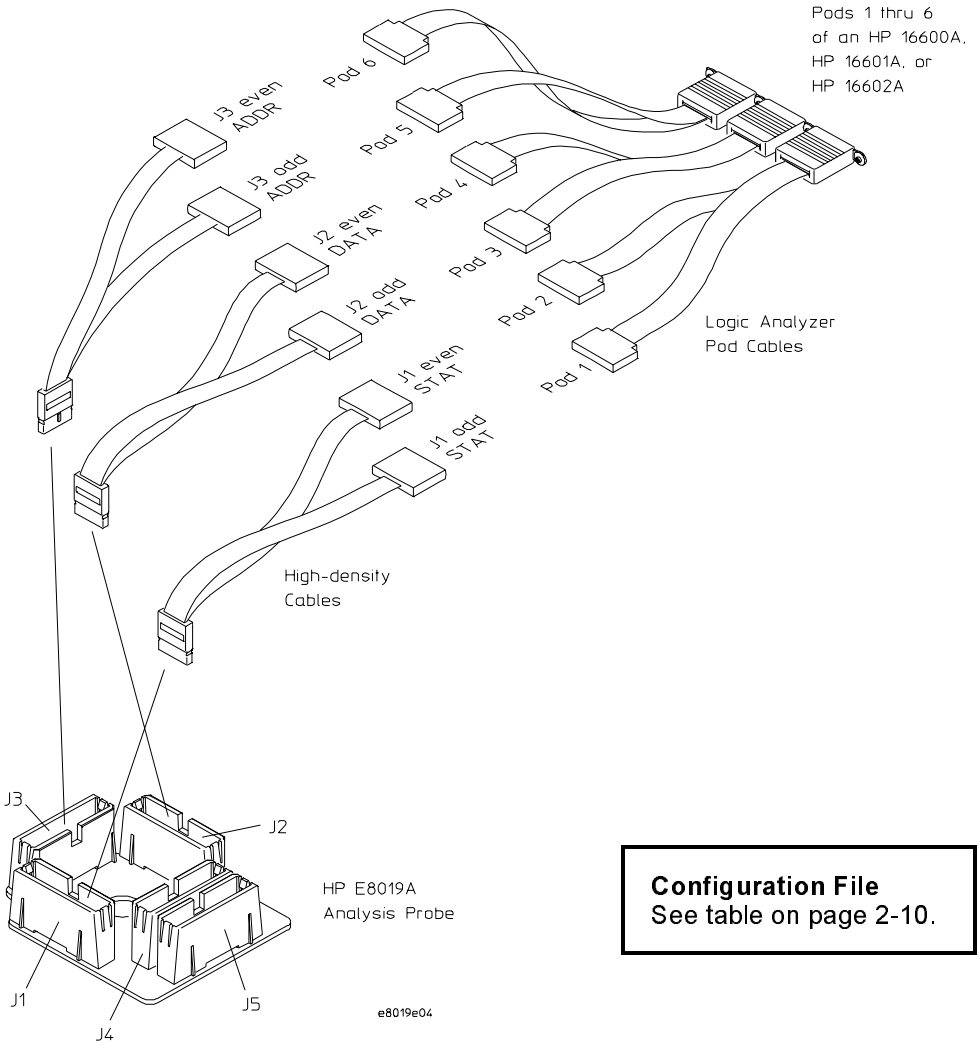
(*2) You may use any memory combinations under the bus speed of 50MHz using 16557.
Condition of <=50MHz : CKIO(cycle) = min20ns, CKIO(low)=min7.5ns, CKIO(high)=min7.5ns

Note

If your 16700A Logic Analyzer equips with three card analyzer (One master, and two slave modules) and your connection type is either "C" or "F", you must detach one of the slave module on your logic analyzer. (One master, and one slave) Refer to the analyzer manual for the instruction on how to detach the module.

Connection Type 'A'
To connect to the HP 16600/1/2A analyzer

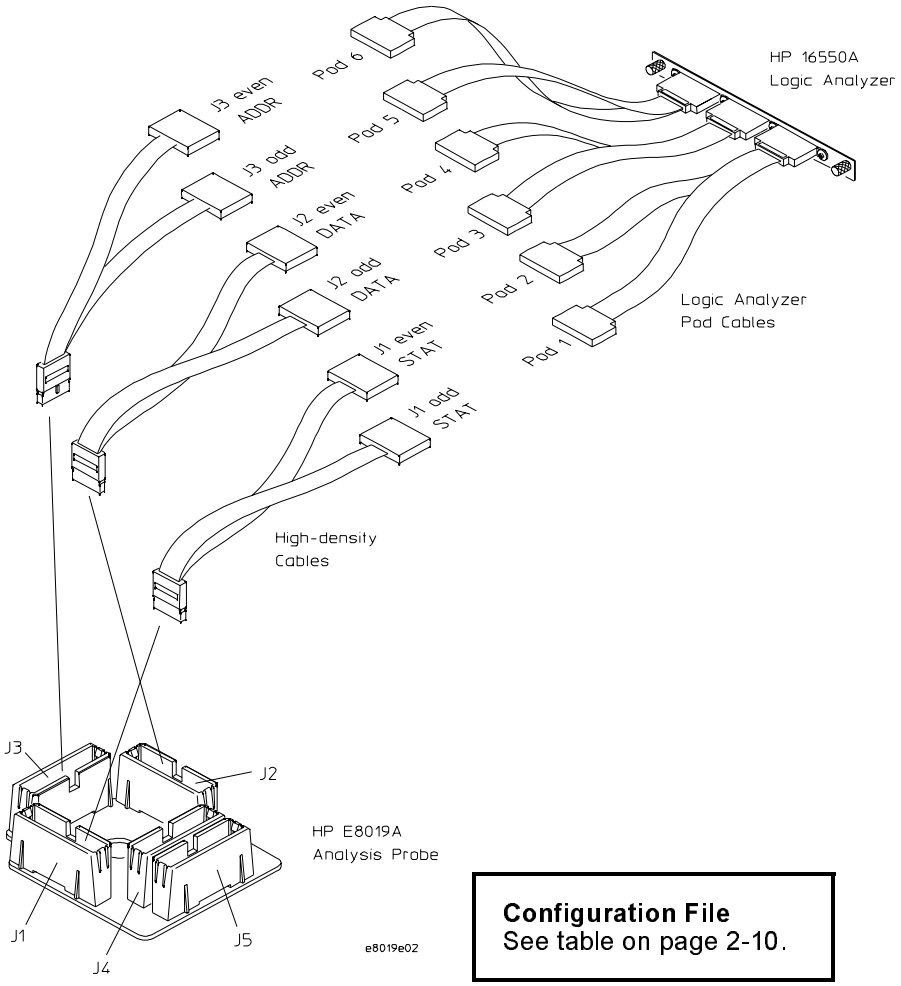
Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

Connection Type 'B'
To connect to the HP 16550A one-card analyzer

Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).

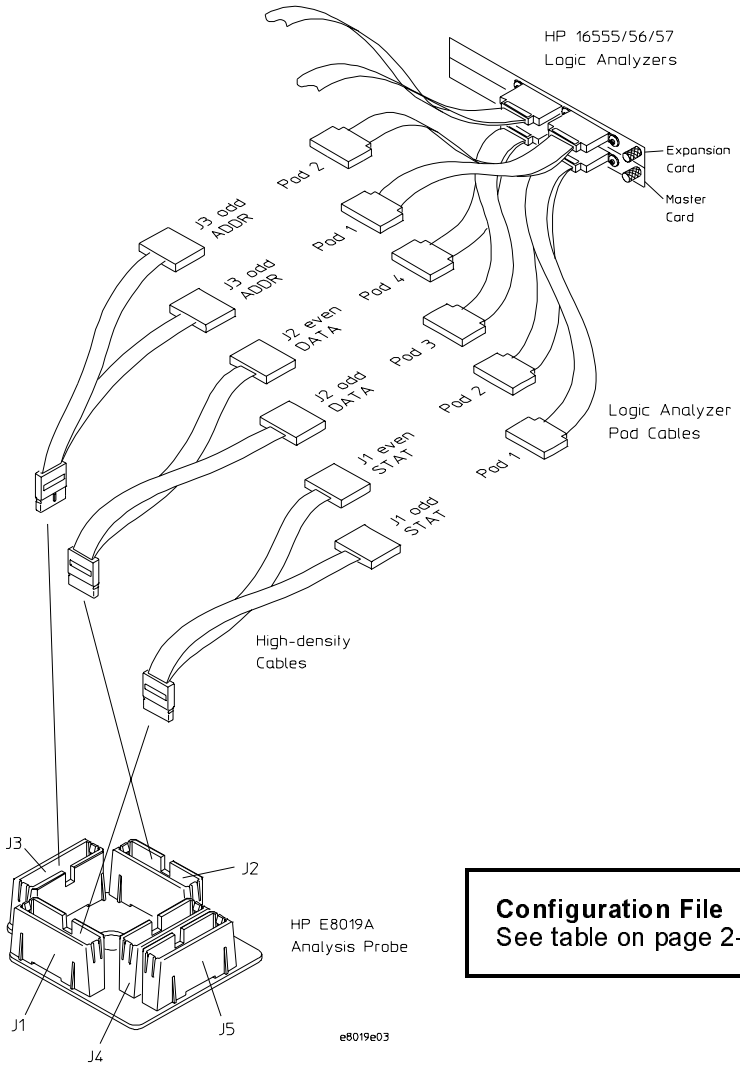


Configuration File
See table on page 2-10.

If your analyzer equips two cards of 16550A, connect all the cables above to "Master" module.

Connection Type 'C'
To connect to the HP 16555/56/57A two-cards analyzer

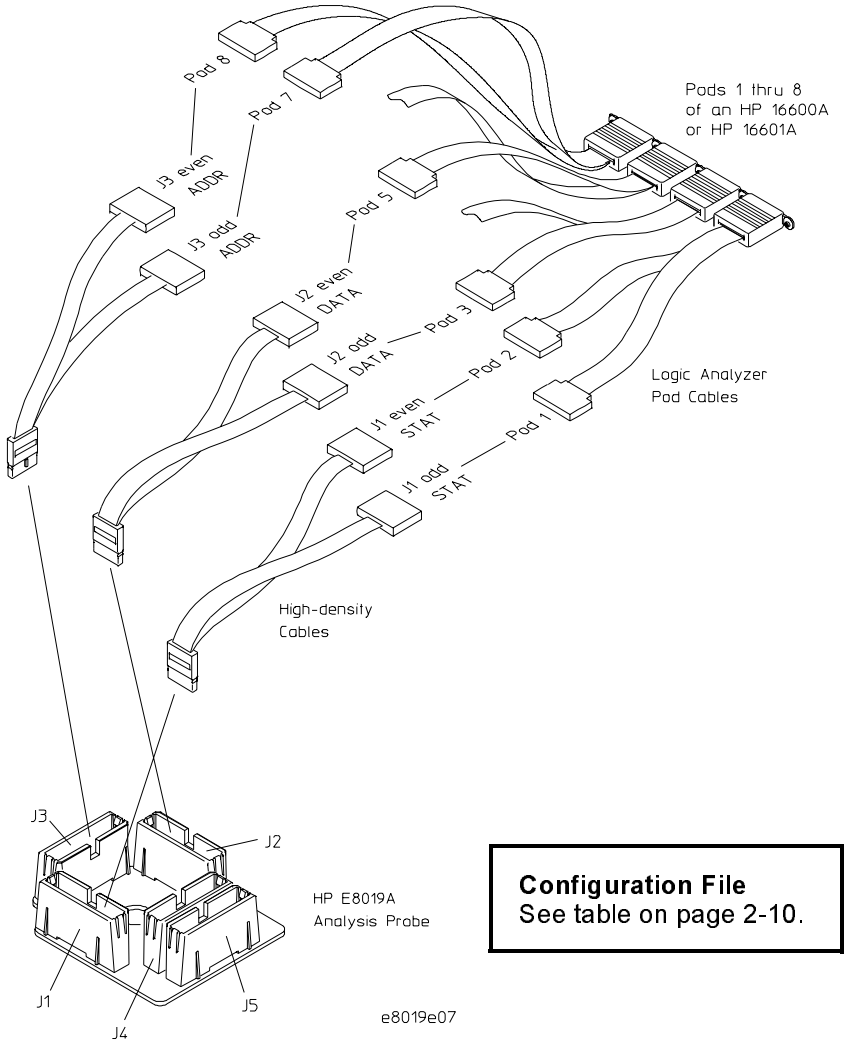
Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

Connection Type 'D'
To connect to the HP 16600/1A analyzer

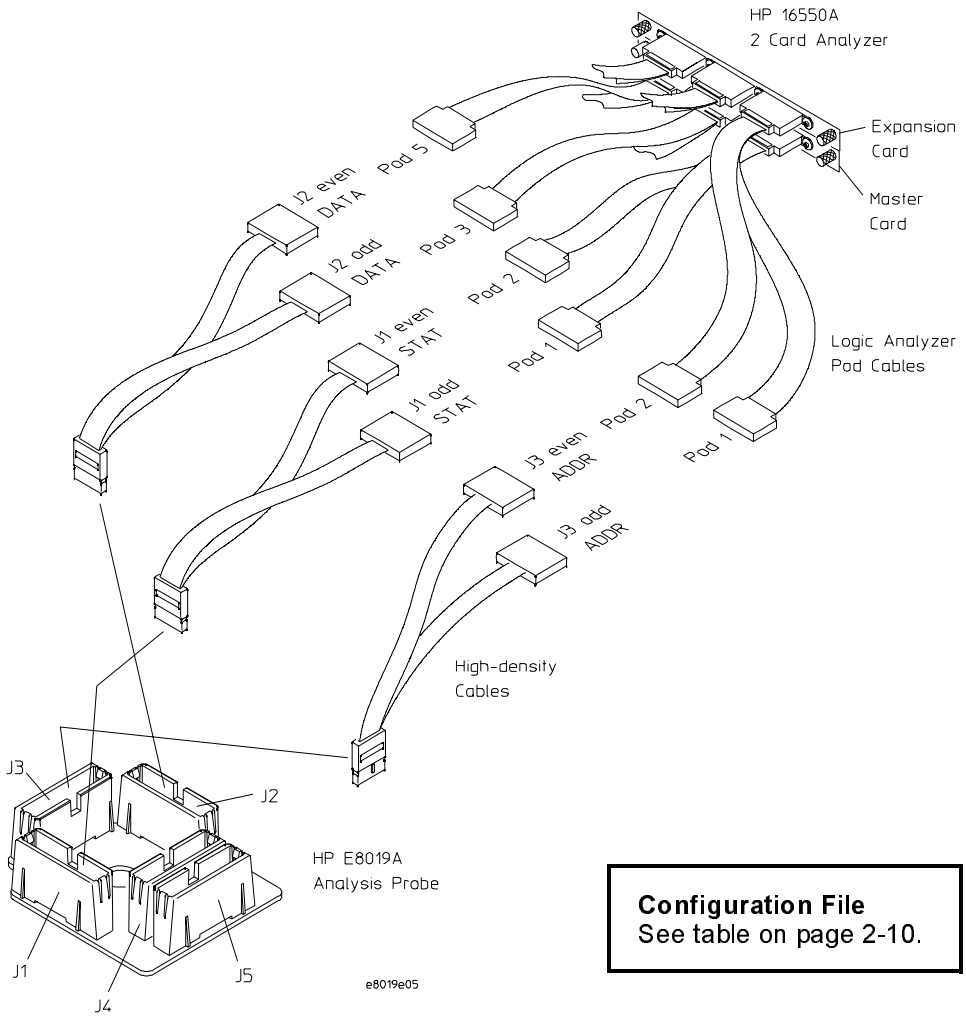
Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

Connection Type 'E'
To connect to the HP 16550A two-cards analyzer

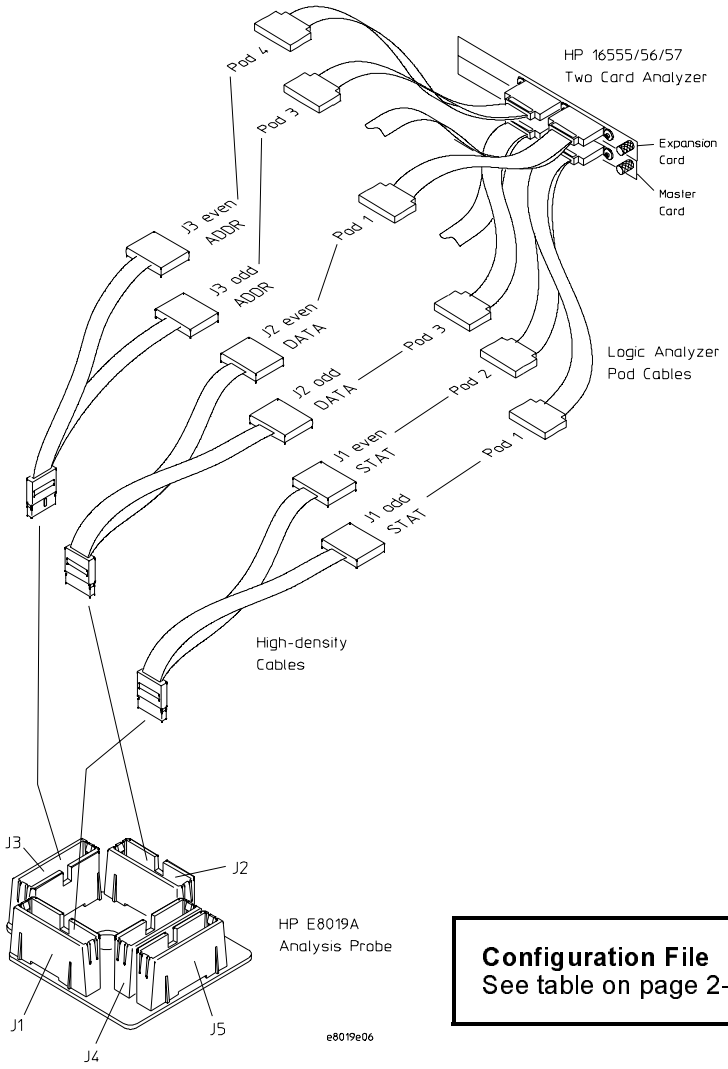
Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

Connection Type 'F'
To connect to the HP 16555/56/57A two-cards analyzer

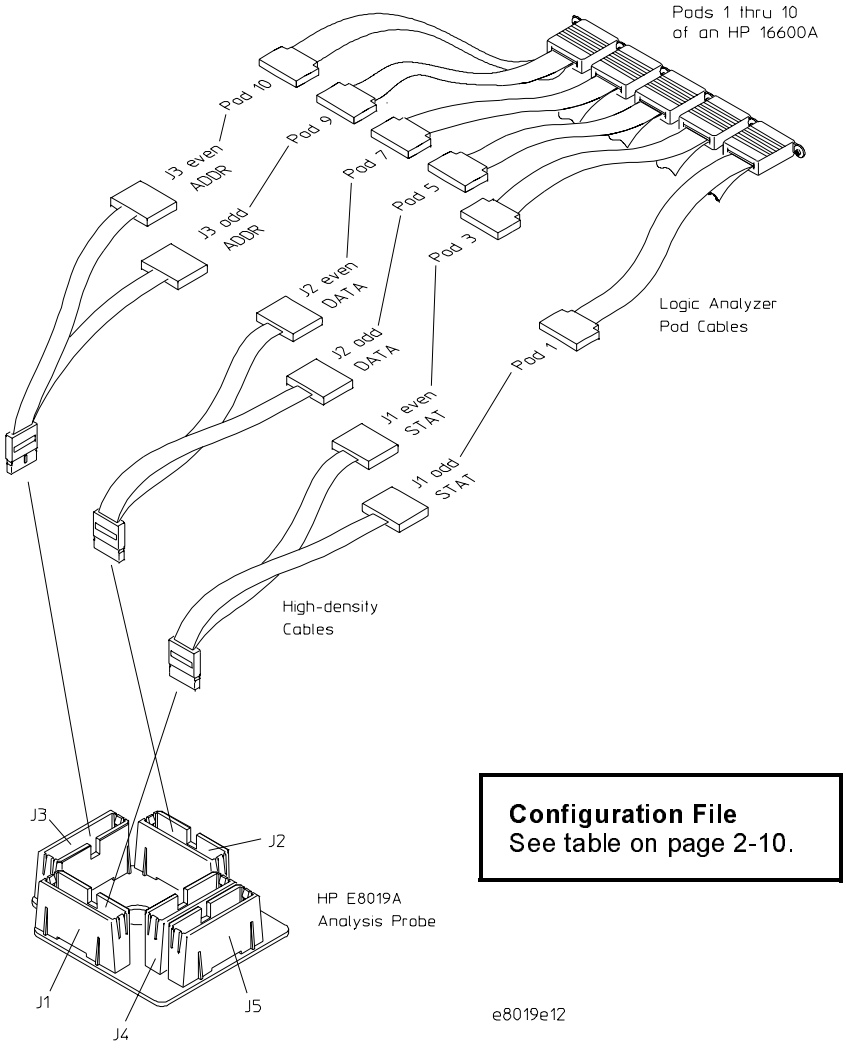
Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

Connection Type 'G'
To connect to the HP 16600A analyzer

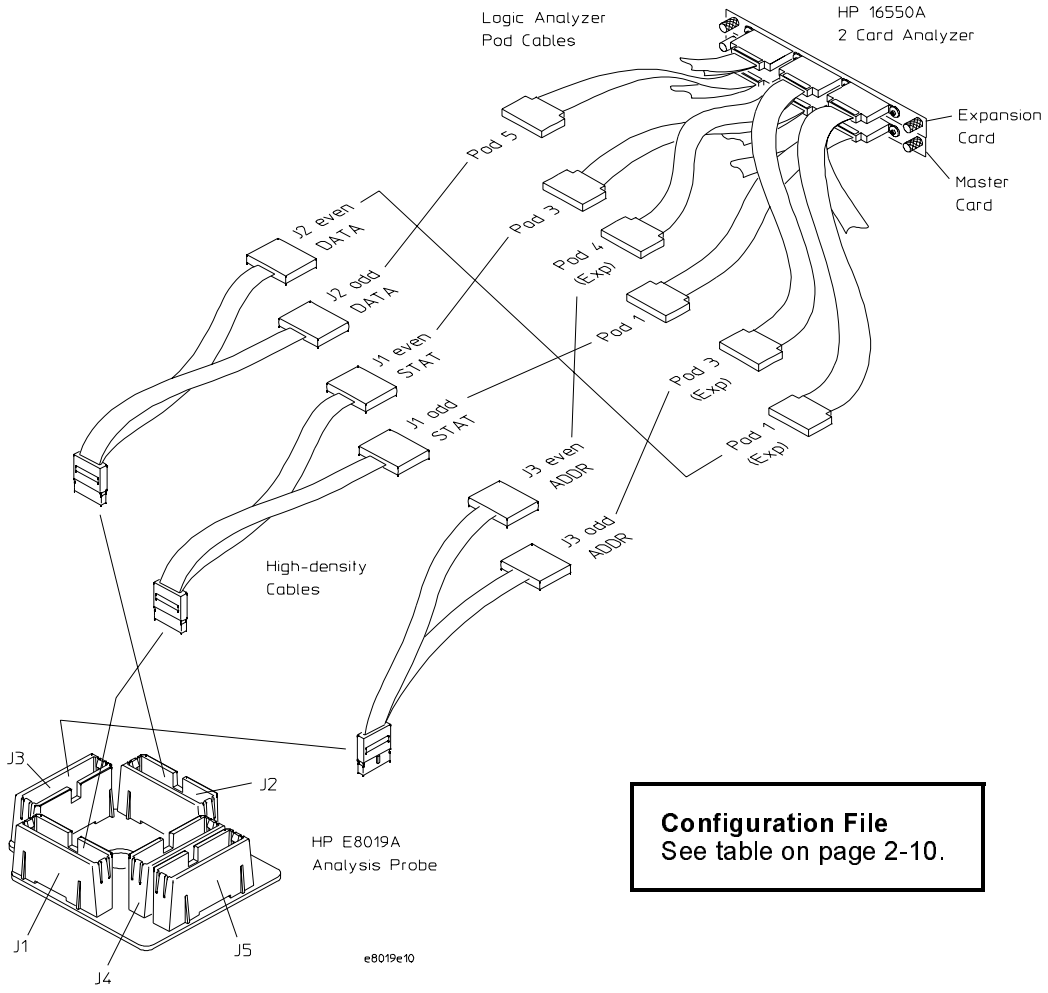
Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

Connection Type 'H'
To connect to the HP 16550A two-cards analyzer

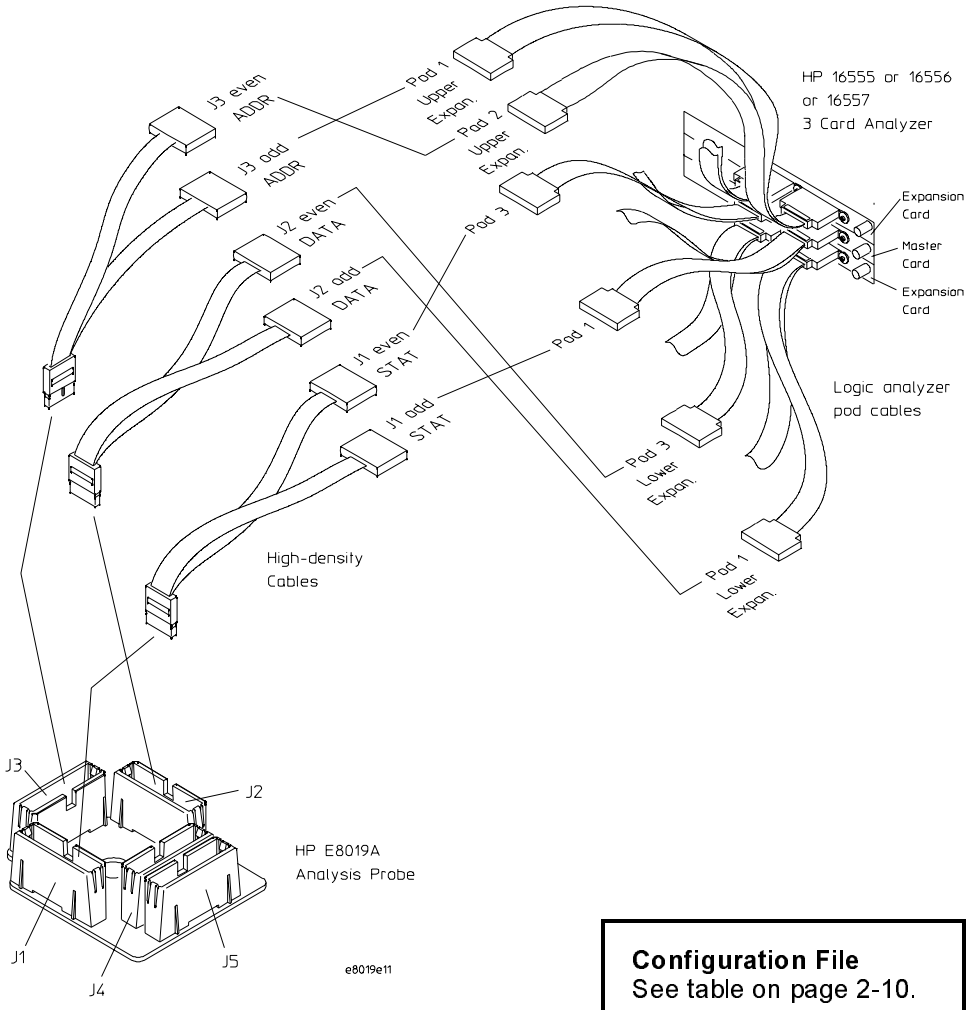
Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

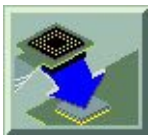
Connection Type 'I'
To connect to the HP 16555/56/57A three-cards analyzer

Connect the pod cables to the Analysis Probeaccording to the pod diagram below (continued on next page).



Configuration File
See table on page 2-10.

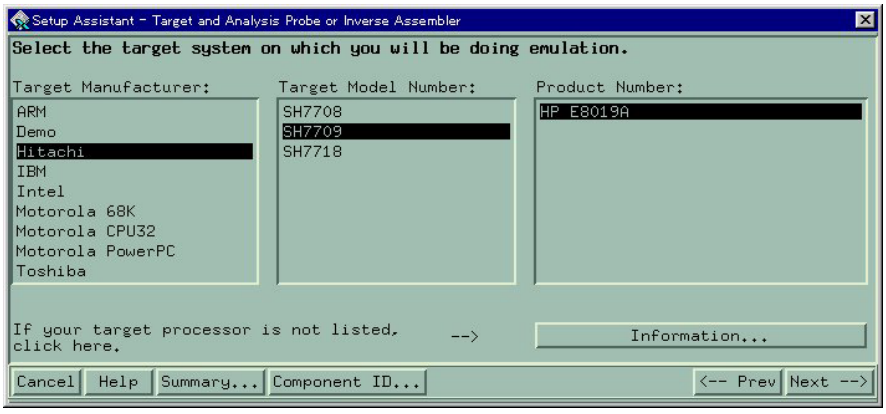
Setup Assistant



The Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. The Setup Assistant is available on the HP 16600A and HP 16700A-series logic analysis systems. You can use the Setup Assistant in place of the connection and configuration procedures provided in this manual.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an Analysis Probe, an emulation module, or other supported equipment. It will also guide you through connecting an Analysis Probeto the target system.

Start the Setup Assistant by clicking its icon in the system window.



If you ordered this Analysis Probeor emulation solution with your HP 16600A/700A-series logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, see the "Installing Software" chapter (page 1).

CAUTION

All operations must be done on the HP-B3759A(HP Emulation Interface Software) except for the MSA.

After finishing MSA, don't touch anything on the state analysis listing window, although it pops up. Any changing on this window migt cause a fatal error on a HP-B3759A(HP Emulation Interface Software).

You can still operate other modules like analog scope. Also as long as you don't remove a state analysis machine, you can operate a workspace to perform cross domain measurement.

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This chapter contains reference information on the HP E8019A hardware including product, electrical, and environmental characteristics, signal mapping, circuit board dimensions, and repair information.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the Analysis Probe.

Product Characteristics

Microcontroller Supported	Hitachi SH7709,7709S,7709R
Package Supported	208-pin TQFP
Pods Required	6,8,or 10logic analyzer pods (three high-density adapter cables) are required for disassembly depending on your target system's memory Two high-density adapter cables are available for additional signal analysis.

Electrical Characteristics

Power Requirements	None.
Signal Line Loading	10pF, 100 kohms on all signals.

Environmental Characteristics

Temperature	Operating	0 to + 50 degrees C +32 to +131 degrees F
Altitude	Operating	4,600 m 15,000 feet
Humidity	Up to 75% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.	

Signal-to-Connector Mapping

The following table shows the the Analysis Probe PGA socket pin mapping.

Table 3-1

SH7709 Signal List

Connector	Analyzer Bit	SH7709 Pin #	Signal Name	Analyzer Label	Analyzer Label
J1odd (6)	CLK1	105	CKE/PTK[5]		
J1odd (8)	15	104	CE2B/PTE[5]		
J1odd (10)	14	103	CE2A/PTE[4]		
J1odd (12)	13	102	CS6/CS1B		
J1odd (14)	12	101	CS5/CE1A/PTK[3]		
J1odd (16)	11	100	CS4/PTK[2]		
J1odd (18)	10	99	CS3/PTK[1]		
J1odd (20)	9	98	CS2/PTK[0]		
J1odd (22)	8		EP-STAT		
J1odd (24)	7	96	CS0		
J1odd (26)	6	93	RDWR		
J1odd (28)	5	92	WE3/DQMUU/ICIOWR/PTK[7]		
J1odd (30)	4	91	WE2/DQMUL/ICIORD/PTK[6]		
J1odd (32)	3	90	WE1/DQMLU/WE		
J1odd (34)	2	89	WE0/DQMLL		
J1odd (36)	1	88	RD		
J1odd (38)	0	87	BS/PTK[4]		
J1even (5)	CLK1	162	CKIO		
J1even (7)	15	126	IOIS16/PTG[7]		
J1even (9)	14	123	WAIT		
J1even (11)	13	122	BREQ		
J1even (13)	12	121	BACK		
J1even (15)	11	119	RAS2U/PTE[1]		
J1even (17)	10	118	RAS3U/PTE[2]		
J1even (19)	9	117	CAS2H/PTE[3]		
J1even (21)	8	116	CAS2L/PTE[6]		
J1even (23)	7	158	STATUS1/PTJ[7]		
J1even (25)	6	157	STATUS0/PTJ[6]		
J1even (27)	5	113	CASHH/PTJ[5]		
J1even (29)	4	112	CASHL/PTJ[4]		
J1even (31)	3	110	CASLH/PTJ[3]		
J1even (33)	2	108	CASLL/CAS/PTJ[2]		
J1even (35)	1	107	RAS2L/PTJ[1]		
J1even (37)	0	106	RAS3L/PTJ[0]		

Connector	Analyzer Bit	SH7709 Pin #	Signal Name	Analyzer Label	Analyzer Label
J2odd (6)	CLK1	124	RESETM		
J2odd (8)	15	34	D15		
J2odd (10)	14	36	D14		
J2odd (12)	13	37	D13		
J2odd (14)	12	38	D12		
J2odd (16)	11	39	D11		
J2odd (18)	10	40	D10		
J2odd (20)	9	41	D9		
J2odd (22)	8	42	D8		
J2odd (24)	7	43	D7		
J2odd (26)	6	44	D6		
J2odd (28)	5	46	D5		
J2odd (30)	4	48	D4		
J2odd (32)	3	49	D3		
J2odd (34)	2	50	D2		
J2odd (36)	1	51	D1		
J2odd (38)	0	52	D0		
J2even (5)	CLK1	193	RESETP		
J2even (7)	15	13	D31/PTB[7]		
J2even (9)	14	14	D30/PTB[6]		
J2even (11)	13	15	D29/PTB[5]		
J2even (13)	12	16	D28/PTB[4]		
J2even (15)	11	17	D27/PTB[3]		
J2even (17)	10	18	D26/PTB[2]		
J2even (19)	9	20	D25/PTB[1]		
J2even (21)	8	22	D24/PTB[0]		
J2even (23)	7	23	D23/PTA[7]		
J2even (25)	6	24	D22/PTA[6]		
J2even (27)	5	25	D21/PTA[5]		
J2even (29)	4	26	D20/PTA[4]		
J2even (31)	3	28	D19/PTA[3]		
J2even (33)	2	30	D18/PTA[2]		
J2even (35)	1	31	D17/PTA[1]		
J2even (37)	0	32	D16/PTA[0]		

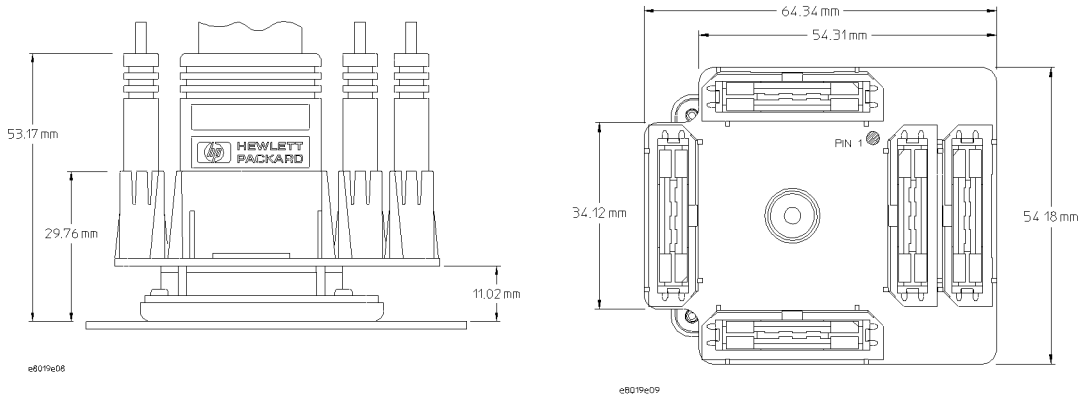
Connector	Analyzer Bit	SH7709 Pin #	Signal Name	Analyzer Label	Analyzer Label
J3odd (6)	CLK1	160	IRQOUT		
J3odd (8)	15	72	A15		
J3odd (10)	14	70	A14		
J3odd (12)	13	68	A13		
J3odd (14)	12	67	A12		
J3odd (16)	11	66	A11		
J3odd (18)	10	65	A10		
J3odd (20)	9	64	A9		
J3odd (22)	8	63	A8		
J3odd (24)	7	62	A7		
J3odd (26)	6	61	A6		
J3odd (28)	5	60	A5		
J3odd (30)	4	58	A4		
J3odd (32)	3	56	A3		
J3odd (34)	2	55	A2		
J3odd (36)	1	54	A1		
J3odd (38)	0	53	A0		
J3even (5)	CLK1	115	DACK1/PTD[7]		
J3even (7)	15	114	DACK0/PTD[5]		
J3even (9)	14	11	IRQ3/IRL3/PTH[3]		
J3even (11)	13	10	IRQ2/IRL2/PTH[2]		
J3even (13)	12	9	IRQ1/IRL1/PTH[1]		
J3even (15)	11	8	IRQ0/IRL0/PTH[0]		
J3even (17)	10	7	NMI		
J3even (19)	9	86	A25		
J3even (21)	8	84	A24		
J3even (23)	7	82	A23		
J3even (25)	6	80	A22		
J3even (27)	5	78	A21		
J3even (29)	4	77	A20		
J3even (31)	3	76	A19		
J3even (33)	2	75	A18		
J3even (35)	1	74	A17		
J3even (37)	0	73	A16		

Connector	Analyzer Bit	SH7709 Pin #	Signal Name	Analyzer Label	Analyzer Label
J4odd (6)	CLK1	159	TCLK/PTH[7]		
J4odd (8)	15	207	AN[7]/DA[0]/PTL[7]		
J4odd (10)	14	206	AN[6]/DA[1]/PTL[6]		
J4odd (12)	13	204	AN[5]/PTL[5]		
J4odd (14)	12	203	AN[4]/PTL[4]		
J4odd (16)	11	202	AN[3]/PTL[3]		
J4odd (18)	10	201	AN[2]/PTL[2]		
J4odd (20)	9	200	AN[1]/PTL[1]		
J4odd (22)	8	199	AN[0]/PTL[0]		
J4odd (24)	7	197	MD5		
J4odd (26)	6	196	MD4		
J4odd (28)	5	195	MD3		
J4odd (30)	4	2	MD2		
J4odd (32)	3	1	MD1		
J4odd (34)	2	144	MD0		
J4odd (36)	1	155	XTAL		
J4odd (38)	0	156	EXTAL		
J4even (5)	CLK1	192	DREQ1/PTD[6]		
J4even (7)	15	194	CA		
J4even (9)	14	125	PTH[5]/ADTRG		
J4even (11)	13	12	IRQ4/PTH[4]		
J4even (13)	12	184	PTD[2]/RSTOUT		
J4even (15)	11	182	WAKEUP/PTD[3]		
J4even (17)	10	176	CTS2/IRQ5/SCPT[7]		
J4even (19)	9	174	RxD2/SCPT[4]		
J4even (21)	8	172	RxD1/SCPT[2]		
J4even (23)	7	171	RxD0/SCPT[0]		
J4even (25)	6	170	RTS2/SCPT[6]		
J4even (27)	5	169	SCK2/SCPT[5]		
J4even (29)	4	168	TxD2/SCPT[4]		
J4even (31)	3	167	SCK1/SCPT[3]		
J4even (33)	2	166	TxD1/SCPT[2]		
J4even (35)	1	165	SCK0/SCPT[1]		
J4even (37)	0	164	TxD0/SCPT[0]		

Connector	Analyzer Bit	SH7709 Pin #	Signal Name	Analyzer Label	Analyzer Label
J5odd (6)	CLK1	124	RESETM		
J5odd (8)	15	120	PTE[0]]		
J5odd (10)	14	94	PTE[7]		
J5odd (12)	13	151	PTH[6]		
J5odd (14)	12		EP-STAT		
J5odd (16)	11		Vcc		
J5odd (18)	10	191	DREQ0/PTD[4]]		
J5odd (20)	9	190	DRAK1/PTD[0]		
J5odd (22)	8	189	DRAK0/PTD[1]		
J5odd (24)	7	177	PTC[7]/PINT7		
J5odd (26)	6	178	PTC[6]/PINT6		
J5odd (28)	5	179	PTC[5]/PINT5		
J5odd (30)	4	180	PTC[4]/PINT4		
J5odd (32)	3	185	PTC[3]/PINT0		
J5odd (34)	2	186	PTC[2]/PINT1		
J5odd (36)	1	187	PTC[1]/PINT2		
J5odd (38)	0	188	PTC[0]/PINT3		
J5even (5)	CLK1	193	RESETP		
J5even (7)	15	126	IOIS16/PTG[7]		
J5even (9)	14	127	PTG[6]		
J5even (11)	13	128	PTG[5]		
J5even (13)	12	129	PTG[4]		
J5even (15)	11	130	PTG[3]		
J5even (17)	10	131	PTG[2]		
J5even (19)	9	133	PTG[1]		
J5even (21)	8	135	PTG[0]		
J5even (23)	7	136	PTF[7]/PINT15		
J5even (25)	6	137	PTF[6]/PINT14		
J5even (27)	5	138	PTF[5]/PINT13		
J5even (29)	4	139	PTF[4]/PINT12		
J5even (31)	3	140	PTF[3]/PINT11		
J5even (33)	2	141	PTF[2]/PINT10		
J5even (35)	1	142	PTF[1]/PINT9		
J5even (37)	0	143	PTF[0]/PINT8		

Circuit Board Dimensions

The following figure gives the dimensions for the Analysis Probe assembly. The dimensions are listed in inches and millimeters.



Circuit Board Dimension Digram

Repair Strategy

The repair strategy for this Analysis Probe is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 3-2 **Replaceable Parts**

HP Part Number	Description
E5374A #201	Retainer Kit
E5374-68701	Locator Tool
E5350-23801	Cam Tool
E5374A	Adapter, Elastomeric, 208-pin QFP
E5346A	High-density Adapter Cable

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Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Hewlett-Packard service center..

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and Analysis Probe. Otherwise, you may damage circuitry in the analyzer, Analysis Probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- **Remove and reseat all cables and probes, ensuring that there are no bent pins on the Analysis Probe or poor probe connections.**
- **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive Loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- **Check for loose cables, board connections, and Analysis Probe connections.**
- **Check for bent or damaged pins on the Analysis probe.**

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- **Check your trigger sequencer specification to ensure that it will capture the events of interest.**
- **Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.**

Analysis Probe Problems

This section lists problems that you might encounter when using a Analysis Probe. If the solutions suggested here do not correct the problem, you may have a damaged Analysis Probe. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the Analysis Probe, the microprocessor (if socketed) or the Analysis Probe may not be installed properly, or they may not be making electrical contact.

- **Ensure that you are following the correct power-on sequence for the Logic Analyzer and target system.**

  1 Power up the Logic Analyzer.

  2 Power up the target system.

  If you power up the target system before you power up the Logic Analyzer, interface circuitry in the Analysis Probe may latch up and prevent proper target system operation.

- **Verify that the microprocessor and the Analysis Probe are properly rotated and aligned, so that the index pin on the microprocessor (pin A1) matches the index pin on the Analysis Probe.**

- **Verify that the microprocessor and the Analysis Probe are securely inserted into their respective sockets.**

- **Verify that the logic analyzer cables are in the proper sockets of the Analysis Probe and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- **Do a full reset of the target system before beginning the measurement.**

  Some Analysis Probe designs require a full reset to ensure correct configuration.

- **Ensure that your target system meets the timing requirements of the processor with the Analysis Probe probe installed.**

  See "Capacitive Loading" in this chapter. While Analysis Probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- **Ensure that you have sufficient cooling for the microprocessor.**

  Microprocessors such as the i486, Pentium?, and MC68040 generate substantial heat. This is exacerbated by the active circuitry on the Analysis Probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the Analysis Probe, or system lockup in the microprocessor. All Analysis Probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- **Remove as many pin protectors, extenders, and adapters as possible.**
- **If multiple Analysis Probe solutions are available, use one with lower capacitive loading.**

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- **Change the trigger specification for modules upstream of the one with the problem.**

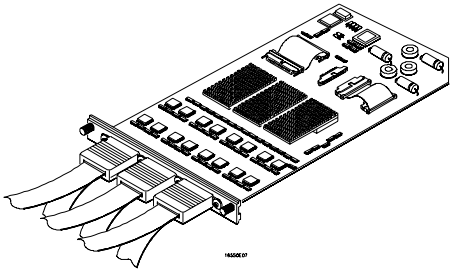
  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Messages

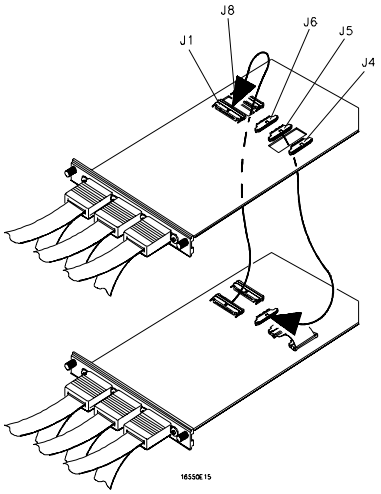
This section lists some of the messages that the analyzer displays when it encounters a problem.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for one or two HP 16550A logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16550A Installations



Cable Connections for Two-Card HP 16550A Installations

See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- **Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most Analysis Probe configuration files.**

See Also Chapter 1 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- **This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/B or HP 16501A frame. Ensure that the cards are firmly seated.**
- **This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.**
- **If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the Analysis Probe. See Chapter 1 to determine the proper connections.**

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- **When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.**

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

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